PRO-LOG
CORPORATION

STD 7000

7503/7506 Optoisolated Input Card

USER'S MANUAL

7503/7506
Optoisolated Input Card
USER'S MANUAL

PRELIMINARY

PRO-LOG
CORPORATION

9/81

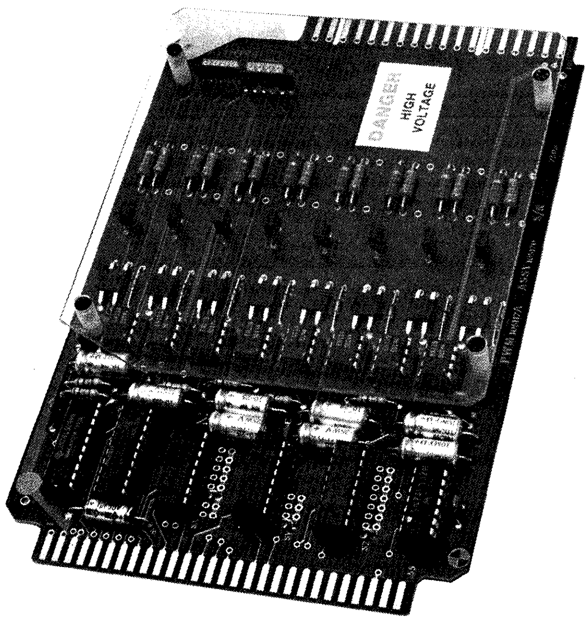
750ISOLATED INPUT CARD USER'S MANUAL

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7000 STD BUS

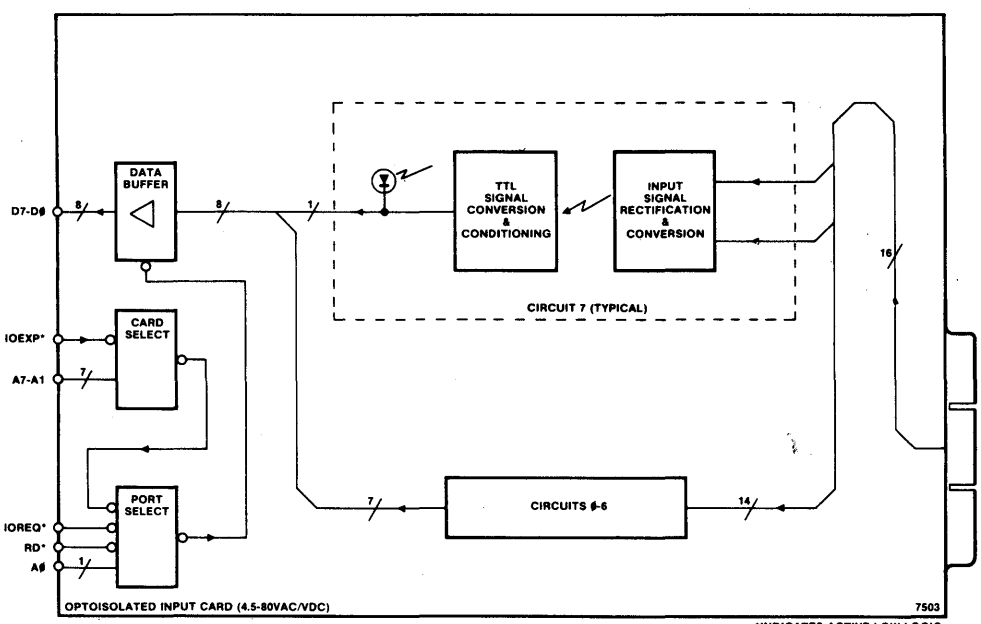
7503 OPTOISOLATED INPUT CARD (4.5-80VAC/VDC)

The 7503 provides eight independent AC/DC inputs for the Series 7000 STD BUS. An optical coupling circuit isolates each circuit from the STD BUS system and from each other. The 7503 offers a choice of two input ranges. Range selection is independent for each input and is selected through the installation of wire jumpers. The low range responds to input voltages between 4.5 VRMS and 22 VRMS for 5V, 6V, and 12V applications. The high range responds to input voltages of between 20 VRMS and 80 VRMS and is useful for systems using 24V, 28V, and 48V. An LED provides a visual indication of the state of each input.



FEATURES

- **500V Minimum Isolation Between Inputs, and Between Each Input and System Ground**
- **Independent Range Selection for Each Input**
- **Low Input Voltage Range from 4.5 VRMS to 22 VRMS**
- **High Input Voltage Range from 20 VRMS to 80 VRMS**
- **10.0mA RMS Maximum Input Loading**
- **Typical Turn On Time of 11msec.**
- **Typical Turn Off Time of 36msec.**
- **LED Indicator for Each Input Circuit**
- **DC Voltages may be Applied with Either Polarity**
- **User-selectable Input Port Address**
- **Keyed Interface Connector**
- **Clear Plastic Safety Shield**
- **Single +5V Operation**
- **Socketed ICs**



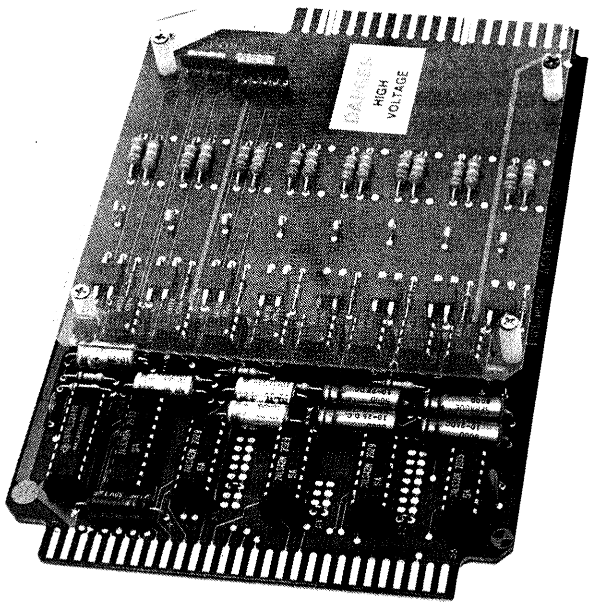
*INDICATES ACTIVE LOW LOGIC

PRO-LOG CORPORATION

7000 STD BUS

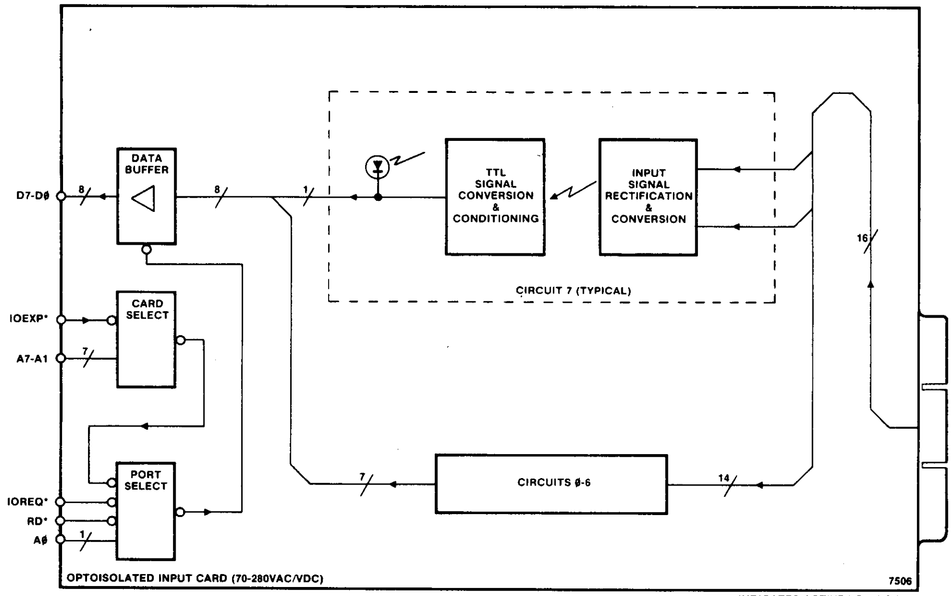
PRELIMINARY 7506
OPTOISOLATED INPUT CARD (70-280VAC/VDC)

The 7506 provides eight independent AC/DC inputs for the Series 7000 STD BUS. An optical coupling circuit isolates each circuit from the STD BUS system and from each other. The 7506 offers a choice of two input ranges. Range selection is independent for each input and is selected through the installation of wire jumpers. The low range responds to input voltages of between 70 VRMS and 150 VRMS for 120V applications. The high range responds to input voltages between 140 VRMS and 280 VRMS and is useful for systems using 240V. An LED provides a visual indication of the state of each input.



FEATURES

- **500V Minimum Isolation Between Inputs, and Between Each Input and System Ground**
- **Independent Range Selection for Each Input**
- **Low Input Voltage Range from 70 VRMS to 150 VRMS**
- **High Input Voltage Range from 140 VRMS to 280 VRMS**
- **2.0mA RMS Maximum Input Loading**
- **Typical Turn On Time of 11msec.**
- **Typical Turn Off Time of 35msec.**
- **LED Indicator for Each Input Circuit**
- **DC Voltages may be Applied with Either Polarity**
- **User-selectable Input Port Address**
- **Keyed Interface Connector**
- **Clear Plastic Safety Shield**
- **Single +5V Operation**
- **Socketed ICs**



*INDICATES ACTIVE LOW LOGIC

PRO-LOG CORPORATION

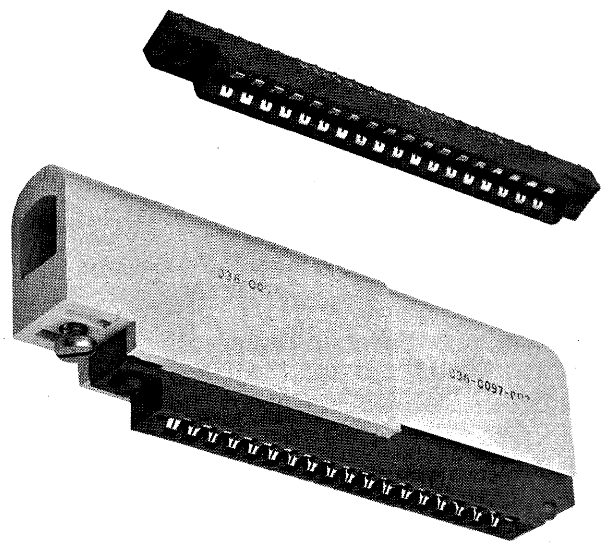
7000 STD BUS I/O EDGE CONNECTOR CS18

SOLDER TAIL CONNECTOR

The CS18 card edge connector is used on industrial interface cards requiring more than 50VDC and/or 0.5A per contact.

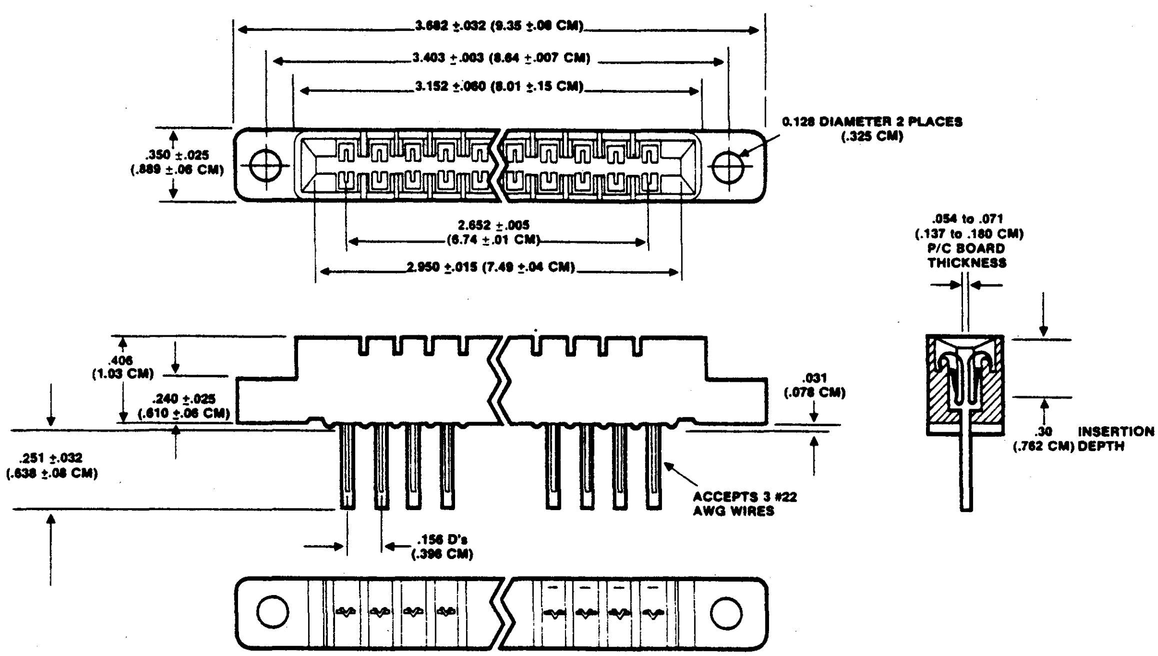
FEATURES

- **5A Maximum Per Contact**
- **Multiple Sourced**
- **Accepts PCBs of .062" Thickness**
- **Pierced Solder Tails Accept 3 #22 AWG Wires**
- **Includes Mating Hood, Hardware, and Keys**
- **UL Listed**



ELECTRICAL

- Material UL rated 94V-0 or 94V-1 (flame rating)
- Contact spacing 0.156" centers
- Contact rating: 5A
- Maximum voltage drop: 30mV at 5A
- Operating voltage: 350V at sea level
- Operating temperature: -55°C to +105°C at sea level
- PCB thickness: .054 to .071 inches
- Insertion/withdrawal forces: 2 oz. to 8 oz. per contact pair



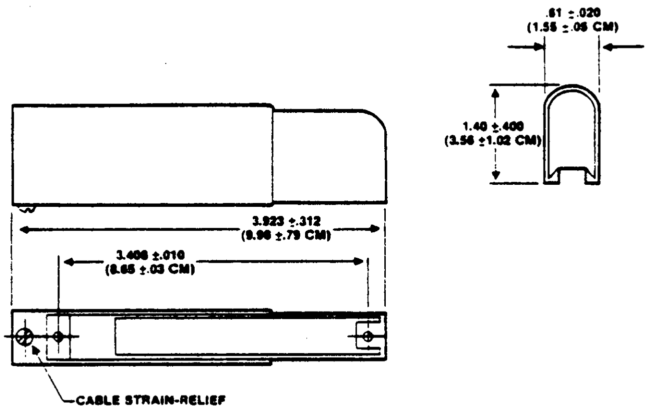
Solder Tail Connector

PRO-LOG CORPORATION

CS18 SOLDER TAIL CONNECTOR

ORDERING INFORMATION

Pro-Log CS18 includes connector, hood, hardware, and key. Part numbers given for other manufacturers are for connectors and hoods only.



Typical Hood with Cable Clamp

Connector

Viking	2VH18/1AB5
Sullins	EMM18 SREH
TRW Cinch	250-18-30-220

Hood

Viking	036-0097-002
Kel-Am	CH-18-6H-3.406
AMP	530088-3

QUANTITY PRICING INFORMATION

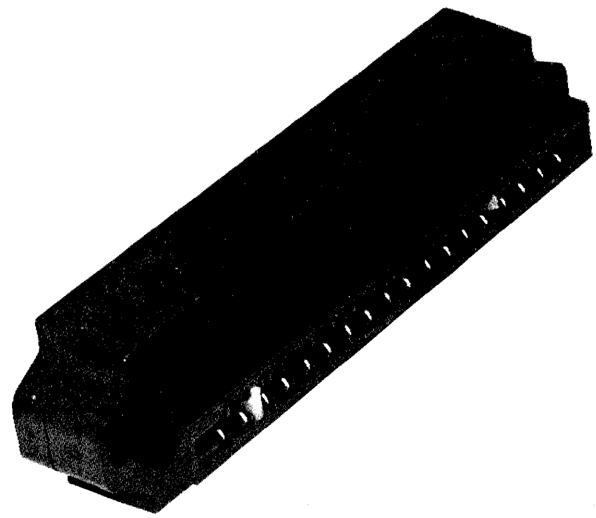
	1 - 9	10 - 24	25 - 99	100 - 249
CS18	$15.00	$13.50	$12.50	$11.50

7000 STD BUS

CB18
I/O EDGE CONNECTOR

BARRIER STRIP CONNECTOR

The CB18 card edge connector is used on industrial interface cards requiring more than 50VDC and/or 0.5A per contact.



FEATURES

- **10A Maximum Per Contact**
- **Single Sourced**
- **Accepts PCBs of .062" Thickness**
- **Tubular Contact Plate Accepts #12 to #22 AWG Wires**
- **Includes Keys**
- **UL Listed**

ELECTRICAL

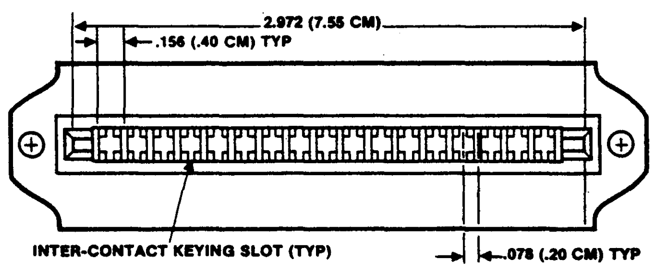
- Material UL rated 94V-0 (flame rating)
- Contact spacing: 0.156" centers
- Contact rating: 10A/circuit continuous
- Breakdown voltage: 2500V
- Operating temperature: -55°C to +105°C at sea level
- PCB thickness: .054 to .071 inches
- Not recommended for more than 20 insertion/withdrawals

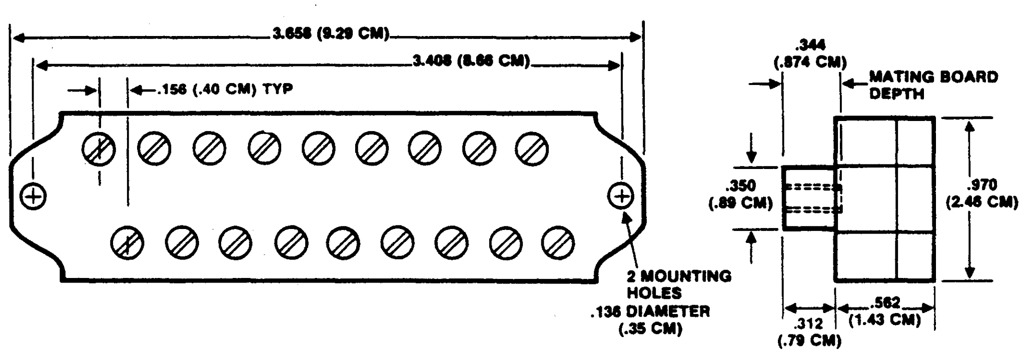
CONNECTOR ORDERING INFORMATION

The part number of various connector manufacturers is given below.

Pro-Log	CB18*
Buchanan	PCB2B Connector
	PC17 Keying plug

*Includes two keying plugs





Barrier Strip Connector

FUNCTIONAL DESCRIPTION

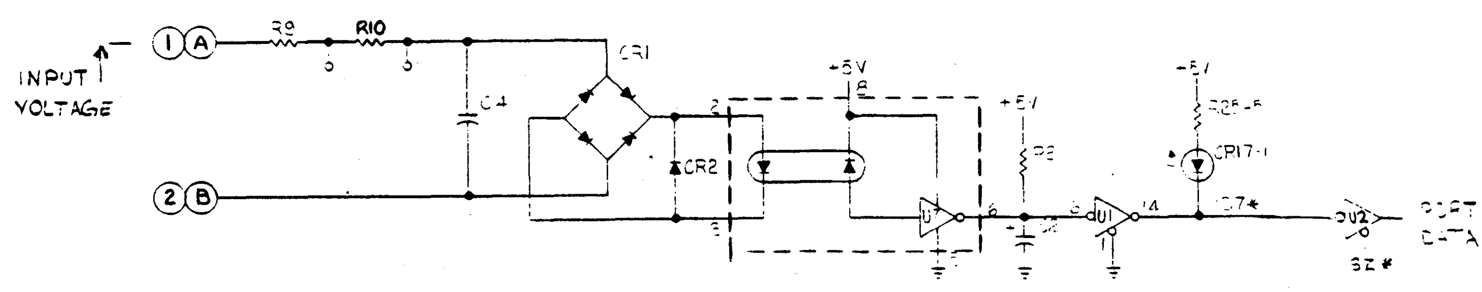
The 7503 and the 7605 Optoisolated Input Cards convert an AC/DC input voltage into a TTL-level signal that is read by an on-card STD BUS input port. The functional operation of the two cards is identical; only component values are changed to permit operation over the wide range of voltages.

The conversion from high voltage to TTL takes place in three steps. A typical input circuit is shown below. The first step uses the input range resistors to obtain a current proportional to the input voltage. The resistor value may be altered for input voltage range selection with the insertion of a jumper wire (jumper in = low range, jumper out = high range). The 7503 is shipped with the jumper out which selects the 20-80 VRMS range. To select the 4.5-22 VRMS range insert the jumper for each circuit desired. The 7506 is also shipped with the jumper out, selecting the 140-280 VRMS range instead of the optional 70-150 VRMS range.

The second step of the conversion process involves full wave rectification of the input current by using a diode bridge. This step allows AC voltages as well as DC voltages of either polarity to be detected.

The third step takes the direct current from the bridge and produces an optically-coupled TTL signal which is read by the input port. The optical coupling provides electrical isolation between the AC circuits and logic circuits of the STD system.

The optoisolated system is free of problems caused by ground loops and varying ground potentials. Analog pulse stretching is provided to assure a constant output signal when a 50Hz or higher frequency AC input signal is applied. This signal is monitored by an LED indicator and the STD BUS input port.



TYPICAL INPUT CIRCUIT

ADDRESS DECODER OPERATION

Refer to the schematics, documents #105119 (7503) or #105298 (7506)

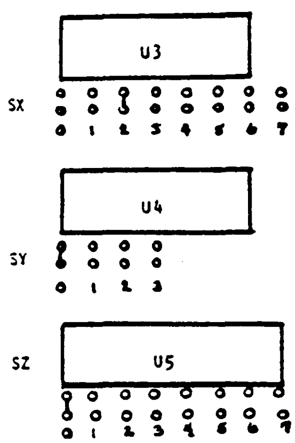
The 7503 and 7506 use three cascaded 74LS42 decoders (U3, U4 and U5) to decode address lines A0-A7. These decoders are enabled only when IORQ*, RD* and IOEXP* are active. The output of the decoder circuit, select signal SZ*, is active only when the card is addressed to read. This signal is used to enable the input port, U2.

CHANGING THE PORT ADDRESS OF THE 7503 AND 7506

Refer to the assembly diagrams, documents #105120 (7503) or #105299 (7506)

Locate decoders U3, U4 and U5 (74LS42) adjacent to the STD BUS edge connector. Each decoder device has a dual row of pads of which form decoder output select matrices. Make one (and only one) connection to each of the matrices adjacent to U3, U4, and U5.

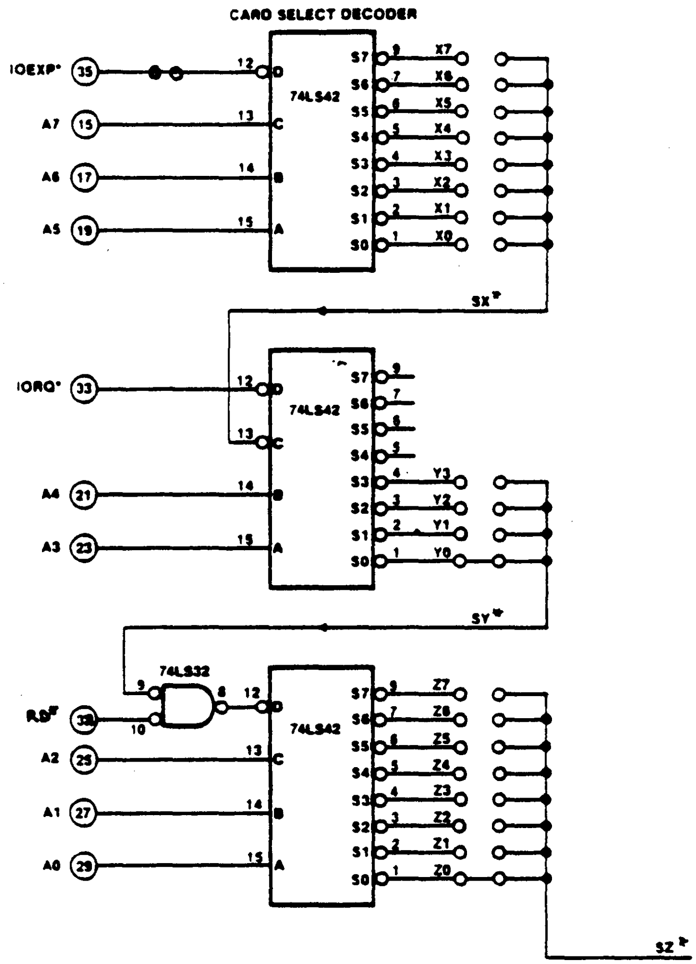
The decoder jumper pad numbering figure shows the numbering of the pads adjacent to the decoder chips on the 7503 and 7506. Also shown are the jumpers (at X2, Y0, and Z0) which produce the hexadecimal port address 40, the selection made when the card is shipped.



The I/O address mapping and jumper selection table for one address per card shows where to place jumper straps to obtain any port address in the hexadecimal range 00-FF. Using the lower of the 2-digit hexadecimal addresses desired, find the most significant hexadecimal address digit along the vertical axis, and the least significant hex digit on the horizontal axis. For example, port address 40 is obtained by connecting jumpers at X2, Y0 and Z0.

The I/O Address Mapping and Jumper Selection Table for one address per card shows where to place jumper straps to obtain any port address in the hexadecimal range 00-FF. Using the lower of the 2-digit hexadecimal addresses desired, find the most significant hexadecimal address digit along the vertical axis, and the least significant hex digit on the horizontal axis. For example, port address 40 is obtained by connecting jumpers at X2, Y0 and Z0.

The pad matrices adjacent to U3, U4 and U5 are on 0.10 inch (0.25cm) centers. The jumper wires may be conveniently replaced by wirewrap post if frequent address selection changes are anticipated.



I/O Address Decoder And Schematic For 1 Address Per Card

MOST SIGNIFICANT HEX ADDRESS	LEAST SIGNIFICANT HEX ADDRESS 0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	JUMPER SELECTION X, Y & Z
	Z0	Z1	Z2	Z3	Z4	Z5	Z6	Z7	Z0	Z1	Z2	Z3	Z4	Z5	Z6	Z7	← Z
0				X0	Y0							X0	Y1				
1				X0	Y2							X0	Y3				
2				X1	Y0							X1	Y1				
3				X1	Y2							X1	Y3				
4				X2	Y0							X2	Y1				
5				X2	Y2							X2	Y3				
6				X3	Y0							X3	Y1				X
7				X3	Y2							X3	Y3				AND
8				X4	Y0							X4	Y1				Y
9				X4	Y2							X4	Y3				
A				X5	Y0							X5	Y1				
B				X5	Y2							X5	Y3				
C				X6	Y0							X6	Y1				
D				X6	Y2							X6	Y3				
E				X7	Y0							X7	Y1				
F				X7	Y2							X7	Y3				

I/O Address Mapping And Jumper Selection Table For 1 Address Per Card

7503 AND 7506 ENVIRONMENTAL SPECIFICATIONS

RECOMMENDED OPERATING LIMITS				ABSOLUTE NON-OPERATING LIMITS		
PARAMETER	MIN	TYP	MAX	MIN	MAX	UNITS
Free Air Temperature	0	25	55	-40	75	°C
Humidity (1)	5		95	0	95	%RH

(1) Non-condensing relative humidity

ELECTRICAL SPECIFICATIONS FOR THE 7503

7503 Optoisolated Input Card Electrical Specifications

MNEM.	PARAMETER	RECOMMENDED OPERATING LIMITS			ABSOLUTE NON-OPERATING LIMITS		
		MIN.	TYP.	MAX.	MIN.	MAX.	UNIT
Vcc	Supply voltage	4.75	5.00	5.25	0.0	7.00	Volt
T_A	Free air temp.	0	25	55	-40	75	°C

User Electrical Characteristics over Recommended Operating Limits

MNEM.	PARAMETER	LOW RANGE			HIGH RANGE			
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	UNIT
V_{IH}	High level user input voltage	4.5		22.0	20.0		80.0	VRMS
V_{IL}	Low level user input voltage	0		3.0	0		3.4	VRMS
I_{IH}	High level user current	0		10.0	.5		2.5	mA
I_{IL}	Low level user input leakage current			14.0			14.0	μamp
R_{IO}	Isolation resistance	10^{10}			10^{10}			Ω
V_{IO}	Isolation voltage	500			500			VDC

STD BUS Electrical Characteristics over Recommended Operating Limits

MNEM.	PARAMETER	LOW RANGE			HIGH RANGE			
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX	UNIT
Icc	STD BUS supply current		150	250		150	250	mA
	STD BUS input load	See STD 7503 Edge Connector Pin List						
	STD BUS output drive	See STD 7503 Edge Connector Pin List						

Switching Characteristics over Recommended Operating Limits

MNEM	PARAMETER	FROM	TO	BOTH RANGES			COMMENTS
				MIN	TYP.	MAX.	
T_{PHL}	Active-Inactive	User Interface	STD Data Bus		36msec.	200msec.	See Timing diagram
T_{PLH}	Inactive-Active	"	"		11msec.	50msec.	See Timing Diagram
T_{STAB}	Stabilize	"	"		50msec.	250msec.	See Timing diagram

ELECTRICAL SPECIFICATIONS FOR THE 7506

7506 Optoisolated Input Card Electrical Specifications

MNEM	PARAMETER	RECOMMENDED OPERATING LIMITS			ABSOLUTE NON-OPERATING LIMITS		
		MIN.	TYP.	MAX.	MIN.	MAX.	UNIT
Vcc	Supply voltage	4.75	5.00	5.25	0.0	7.00	Volt
T_A	Free air temp.	0	25	55	-40	75	°C

User Electrical Characteristics over Recommended Operating Limits

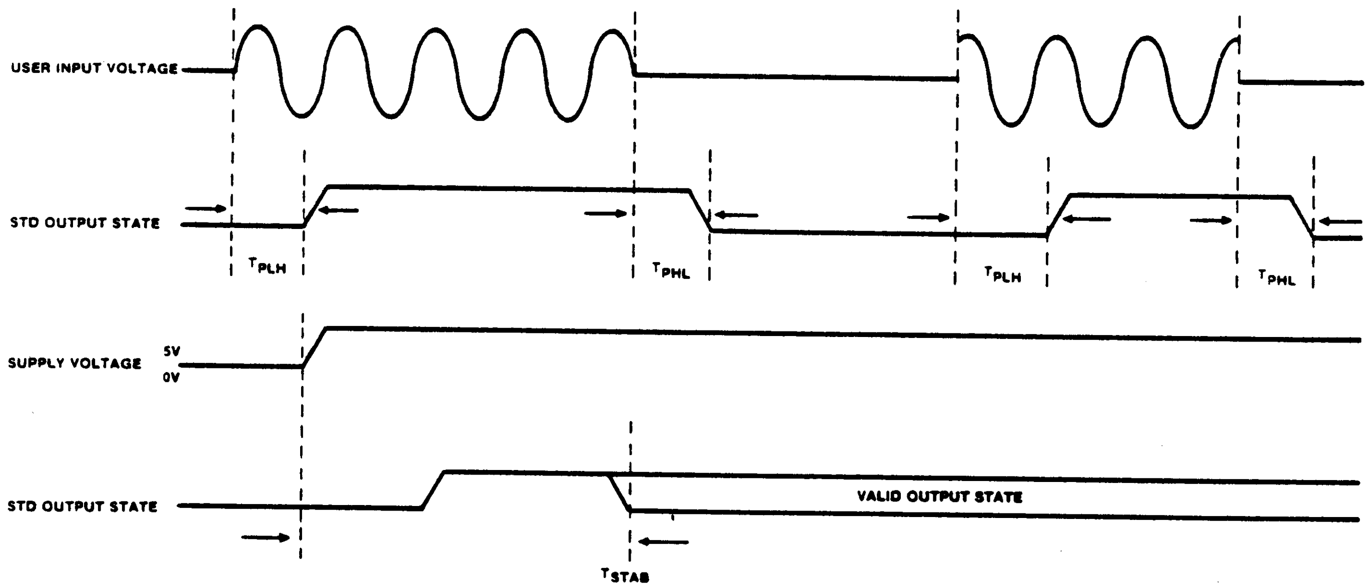
MNEM	PARAMETER	LOW RANGE			HIGH RANGE			
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	UNIT
V_{IH}	High level user input voltage	70		150	140		280	VRMS
V_{IL}	Low level user input voltage			4.0			7.0	VRMS
I_{IH}	High level user input current	.50		2.0	.50		1.0	mA
I_{IL}	Low level user input leakage current			14.0			14.0	μamp
R_{IO}	Isolation resistance	10^{10}			10^{10}			Ω
V_{IO}	Isolation voltage	1500			1500			VDC

STD BUS Electrical Characteristics over Recommended Operating Limits

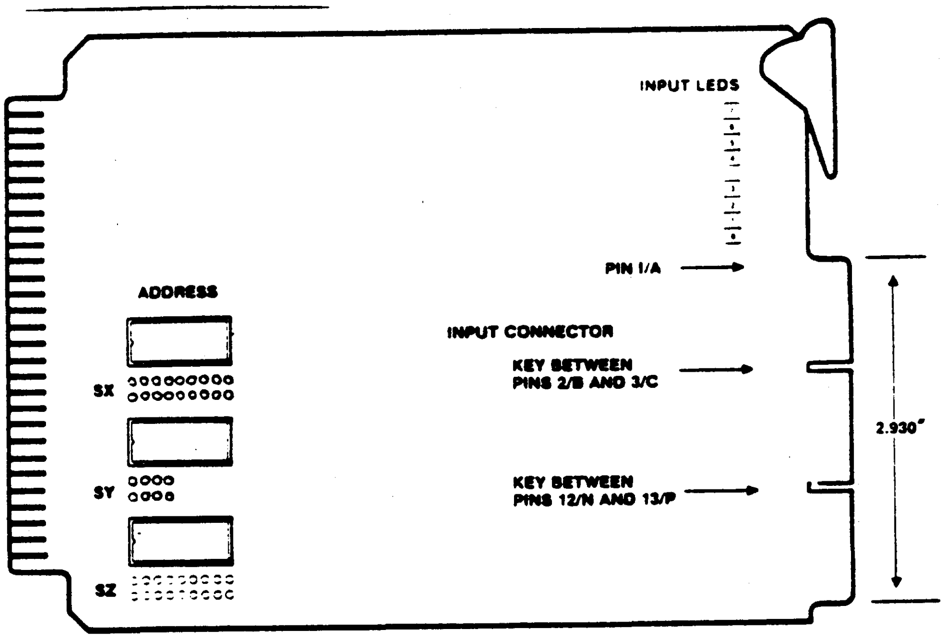
MNEM	PARAMETER	LOW RANGE			HIGH RANGE			
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	UNIT
Icc	STD BUS supply current		150	250		150	250	mA
	STD BUS input load	See STD 7506 Edge Connector Pin List						
	STD BUS output drive	See STD 7506 Edge Connector Pin List						

Switching Characteristics over Recommended Operating Limits

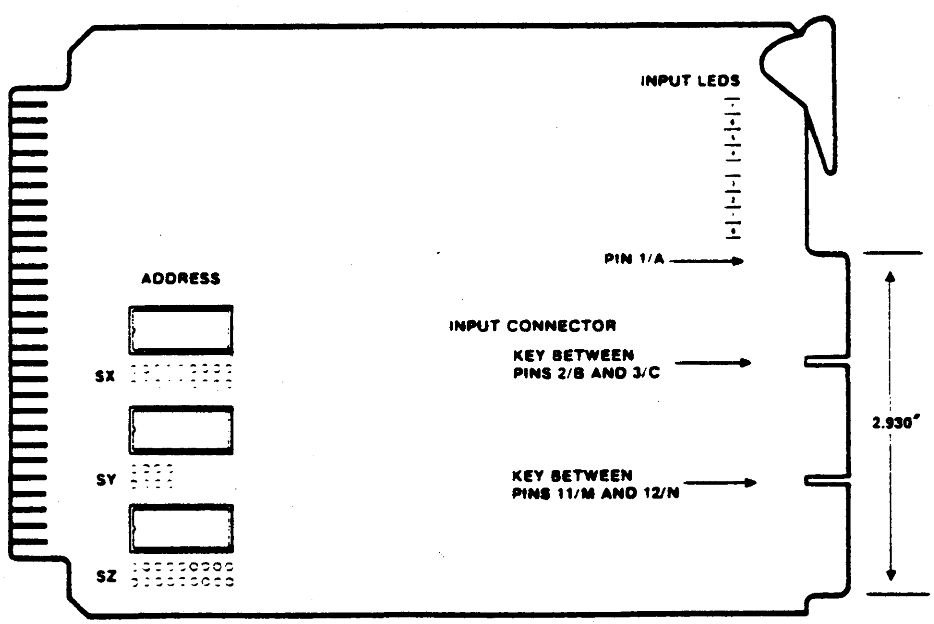
MNEM	PARAMETER	FROM	TO	BOTH RANGES			COMMENTS
				MIN	TYP.	MAX.	
T_{PHL}	Active-Inactive	User Interface	STD Data Bus		36msec.	200msec.	See Timing diagram
T_{PLH}	Inactive-Active	"	"		11msec.	60msec.	See Timing Diagram
T_{STAB}	Stabilize	"	"		50msec.	250msec.	See Timing diagram



INPUT CIRCUIT TIMING DIAGRAM



7503 COMPONENT PLACEMENT DIAGRAM



7506 COMPONENT PLACEMENT DIAGRAM

INTERFACE CONNECTOR PIN LIST	
PIN NUMBER	SIGNAL
1/A	AC INPUT 7A
2/B	7B
3/C	AC INPUT 6A
4/D	6B
5/E	AC INPUT 5A
6/F	5B
7/H	AC INPUT 4A
8/J	4B
9/K	AC INPUT 3A
10/L	3B
11/M	AC INPUT 2A
12/N	2B
13/P	AC INPUT 1A
14/R	1B
15/S	AC INPUT 0A
16/T	0B
17/U	SPARE
18/V	SPARE

7503/7506 **Interface Connector Pin List**

EDGE CONNECTOR PIN LIST							
MNEMONIC	INPUT (LSTTL LOADS)	OUTPUT (LSTTL DRIVE)	PIN NUMBER	PIN NUMBER	OUTPUT (LSTTL DRIVE)	INPUT (LSTTL LOADS)	MNEMONIC
+5 VOLTS	VCC		2	1		VCC	+5 VOLTS
GROUND	GND		4	3		GND	GROUND
-5V			6	5			-5V
D7		55	8	7	55		D3
D6		55	10	9	55		D2
D5		55	12	11	55		D1
D4		55	14	13	55		D0
A15			16	15		1	A7
A14			18	17		1	A6
A13			20	19		1	A5
A12			22	21		1	A4
A11			24	23		1	A3
A10			26	25		1	A2
A9			28	27		1	A1
A8			30	29		1	A0
RD*	1		32	31			WR*
MEMRQ*			34	33		1	IORQ*
MEMEX*			36	35		1	IOEXP*
MCSYNC*			38	37			REFRESH*
STATUS 0*			40	39			STATUS 1*
BUSRQ*			42	41			BUSAK*
INTRQ*			44	43			INTAK*
NMIRQ*			46	45			WAITRQ*
PBRESET*			48	47			SYSRESET*
CNTRL*			50	49			CLOCK*
PCI	IN		52	51	OUT		PC0
AUX GND			54	53			AUX GND
AUX -V			56	55			AUX +V

*Designates Active Low Level Logic

7503/7506 **Edge Connector Pin List**

MECHANICAL

Refer to the Component Placement Diagram for component placement information.

The 7503/7506 meets all STD BUS general mechanical specifications. The 7503/7506 requires clearances of 0.150" on the circuit side and 0.600" on the component side of the printed circuit board when placed in a Series 7000 card rack.

Clear plastic shields are provided on both sides of the assembly for protection from high voltage. Both adjacent slots must be vacant for clearance of the shields and the input connector.

The user can connect the 7503/7506 by using a PC board edge connector with solder tail connections. The recommended card edge connector is supplied with Pro-Log assembly CS18. Also included are a protective hood, all hardware, and keys. The keys must be installed in the position shown in the component placement diagram.

7503 AND 7506 OPERATING SUBROUTINE MODULE

This section provides a flow diagram and subroutine to operate your 7503/7506 card. It may be used intact, or used as a model to construct subroutines for a specific application. The subroutine is written in 8080-family assembly code and will execute on 8080, 8085, and Z80 processors. The memory addresses selected are compatible with Pro-Log's 7801 (8085A) and 7803 (Z80) processor cards. The 7503/7506 port addresses used are the address jumper selections made when the 7503/7506 is shipped.

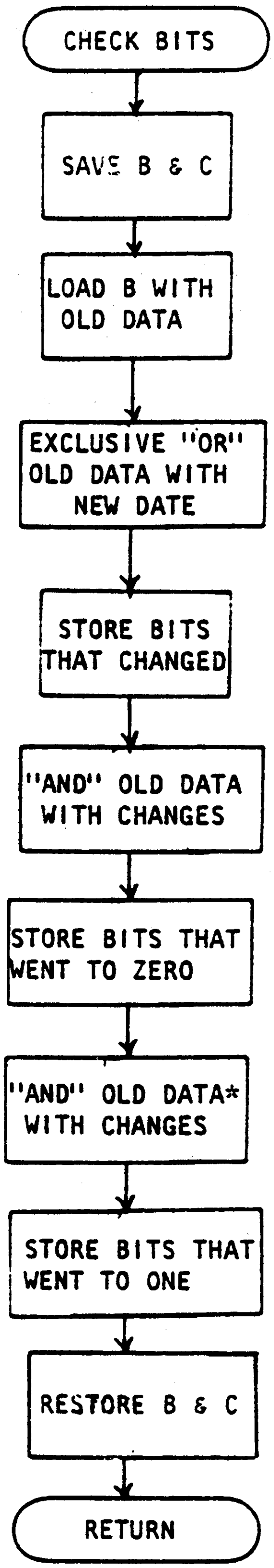
To use the subroutine in systems other than those described above, the memory and/or I/O port addresses may require change for compatibility. The flow diagram presented can be easily translated into the assembly code used by any microprocessor since they show the steps required to acheive 7503/7506 operation without reference to particular microprocessor.

The following subroutine will compare the present port status with the port status from the last time that the port was read. To use the routine the HL pointer must point to a place in memory where port status is stored. Also, the port must be read into the accumulator before calling the routine. Upon return from the routine the location that the HL pointer was previously set will contain new port status. Plus the next four locations will contain change status.

Uses Registers A, C, H and L

M	XX New Data	←Location HL was set to
M + 1	XX Old Data	
M + 2	XX Changes	
M + 3	XX Bits to Zero	
M + 4	XX Bits to One	

Memory after Return


CHECK BITS
SAVE B & C
LOAD B WITH OLD DATA
EXCLUSIVE "OR" OLD DATA WITH NEW DATE
STORE BITS THAT CHANGED
"AND" OLD DATA WITH CHANGES
STORE BITS THAT WENT TO ZERO
"AND" OLD DATA* WITH CHANGES
STORE BITS THAT WENT TO ONE
RESTORE B & C
RETURN

PRO-LOG CORPORATION — **PROGRAM ASSEMBLY FORM**

TITLE 7503/7506 DATE

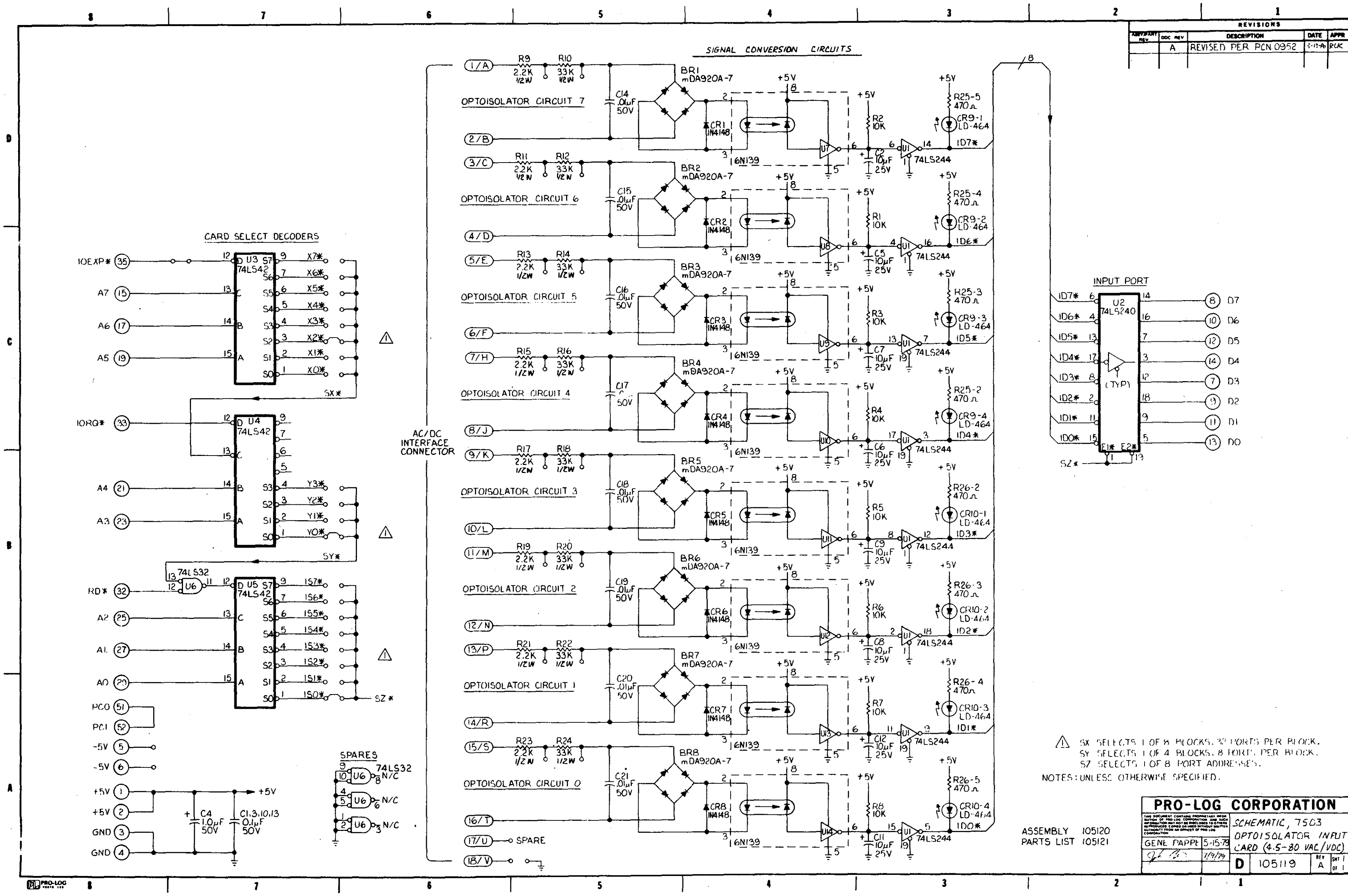
HEXADECIMAL PAGE ADR	LINE ADR	INSTR.	MNEMONIC LABEL	INSTR.	MODIFIER	COMMENTS
	0			LDPI	HL	Set Pointer
	1			—	XX	
	2			—	XX	
	3			IPA		Input New Data
	4			—	XX	
	5	C5	(Check Bits)	PSP	BC	← Save Contence of Regs B and C
	6	46		LDB	M(HL)	← Put OLD Data in B
	7	77		STAN	(HL)	← Store New Data
	8	23		ICP	(HL)	Store OLD Data in Next Location
	9	70		STBN	(HL)	
	A	A8		XRA	B	← OLD ⊕ NEW = CHANGES
	B	23		ICP	HL	Store CHANGES in Next Location
	C	77		STAN	(HL)	
	D	4F		LDC	A	← Put Changes in C
	E	78		LDA	B	← Put OLD DATA IN A
	F	A1		ANA	C	← OLD • CHANGES = Bits to Zero
	0	23		ICP	HL	Store Bits to Zero in Next Location
	1	77		STAN	(HL)	
	2	78		LDA	B	Compliment OLD DATA
	3	2F		CMA		
	4	A1		ANA	C	← $\overline{OLD}$ • CHANGES = Bits to ONE
	5	23		ICP	HL	Store Bits to ONE in Next Location
	6	77		STAN	(HL)	
	7	C1		PLP	BC	← Restore Contence of Reg B and C
	8	C9		RTS	UN	← Return from Subroutine
	9					USES REG A and Pointer HL
	A					
	B					
	C					
	D					
	E					
	F					

	00001111	OLD
⊕	01010101	NEW
	01011010	CHANGES

	00001111	OLD
•	01011010	CHANGES
	00001010	Bits to Zero

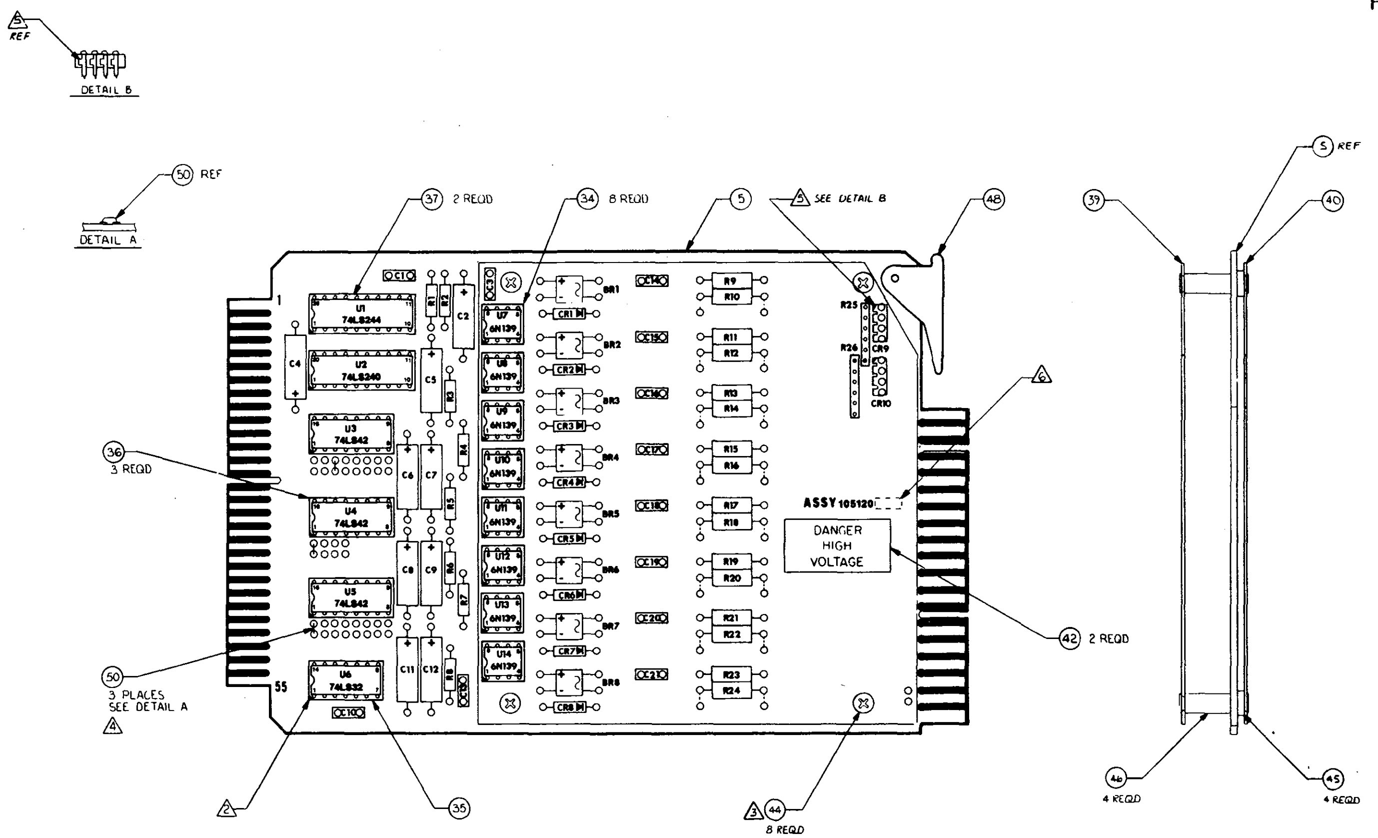
	11110000	$\overline{OLD}$
•	01011010	CHANGES
	01010000	Bits to ONE

RAM MEMORY	XX NEW DATA	M
AFTER Return	XX OLD DATA	M+1
(uses 5 Locations)	XX CHANGES	M+2
	XX Bits to Zero	M+3
	XX Bits to ONE	M+4



REVISIONS
A REVISED PER PCN 0952
SIGNAL CONVERSION CIRCUITS
CARD SELECT DECODERS
IOEXP* 35
A7 15
A6 17
A5 19
U3 74LS42
X7* X6* X5* X4* X3* X2* X1* X0*
SX*
IORQ* 33
U4 74LS42
A4 21
A3 23
Y3* Y2* Y1* Y0*
SY*
74LS32
RD* 32
U5 74LS42
A2 25
A1 27
A0 29
IS7* IS6* IS5* IS4* IS3* IS2* IS1* IS0*
SZ*
PC0 51
PC1 52
-5V 5
-5V 6
+5V 1
+5V 2
GND 3
GND 4
C4 1.0μF 50V
C1,3,10,13 0.1μF 50V
SPARES
74LS32
U6 N/C
AC/DC INTERFACE CONNECTOR
OPTOISOLATOR CIRCUIT 7
OPTOISOLATOR CIRCUIT 6
OPTOISOLATOR CIRCUIT 5
OPTOISOLATOR CIRCUIT 4
OPTOISOLATOR CIRCUIT 3
OPTOISOLATOR CIRCUIT 2
OPTOISOLATOR CIRCUIT 1
OPTOISOLATOR CIRCUIT 0
1/A 2/B 3/C 4/D 5/E 6/F 7/H 8/J 9/K 10/L 11/M 12/N 13/P 14/R 15/S 16/T 17/U 18/V
SPARE
R9 2.2K 1/2W
R10 33K 1/2W
C14 .01μF 50V
BR1 mDA920A-7
CR1 1N4148
6N139
+5V
R2 10K
C2 10μF 25V
74LS244
R25-5 470Ω
CR9-1 LD-464
ID7* ID6* ID5* ID4* ID3* ID2* ID1* ID0*
INPUT PORT
U2 74LS240
(TYP)
D7 D6 D5 D4 D3 D2 D1 D0
SX SELECTS 1 OF 8 BLOCKS, 32 PORTS PER BLOCK.
SY SELECTS 1 OF 4 BLOCKS, 8 PORTS PER BLOCK.
SZ SELECTS 1 OF 8 PORT ADDRESSES.
NOTES: UNLESS OTHERWISE SPECIFIED.
ASSEMBLY 105120
PARTS LIST 105121
PRO-LOG CORPORATION
SCHEMATIC, 7503 OPTOISOLATOR INPUT CARD (4.5-30 VAC/VDC)
GENE PAPPE 5-15-79
D 105119 A

REVISIONS				
ASSY/PORT REV	DOC REV	DESCRIPTION	DATE	APPR
	A	REVISED PER PCN 0952		
	B	REVISED PER PCN .140		



7. REF DESIGNATIONS ARE FOR LOCATING PURPOSES ONLY AND MAY NOT APPEAR ON ACTUAL PART.
6 IDENTIFY WITH ASSY REV LETTER USING RUBBER STAMP.
5 *INDICATES CATHODE PIN OF LED (TYP)*
4 MAPPED TO PORT 40.
3 APPLY LOCKTITE TO SCREWS.
2 DENOTES PIN 1 END OF IC'S.
1. BOARD TO CONFORM WITH ASSEMBLY STANDARD AS1004.
NOTES: UNLESS OTHERWISE SPECIFIED.

SCHEMATIC 105119
PARTS LIST 105121

ITEM	DESCRIPTION	REF. DESIGNATION
24	33K, CF, 1/2 W, 5%	R10,12,14,16,18,20,22,24
23	2.2K, CF, 1/2 W, 5%	R9,11,13,15,17,19,21,23
22	470Ω NETWORK	R25-26
21	10K, CF, 1/4W, 5%	R1-8
17	MDA920A-7	BR1-8
16		
15	1N4148	CR1-8
14		
13	LD464	CR9,10
12		
11	10uF 25V	[illegible]
10	1μF 50V	C4
9		
8	.1μF 50V	C1,3,10,13
7	.01μF 50V	C14-21

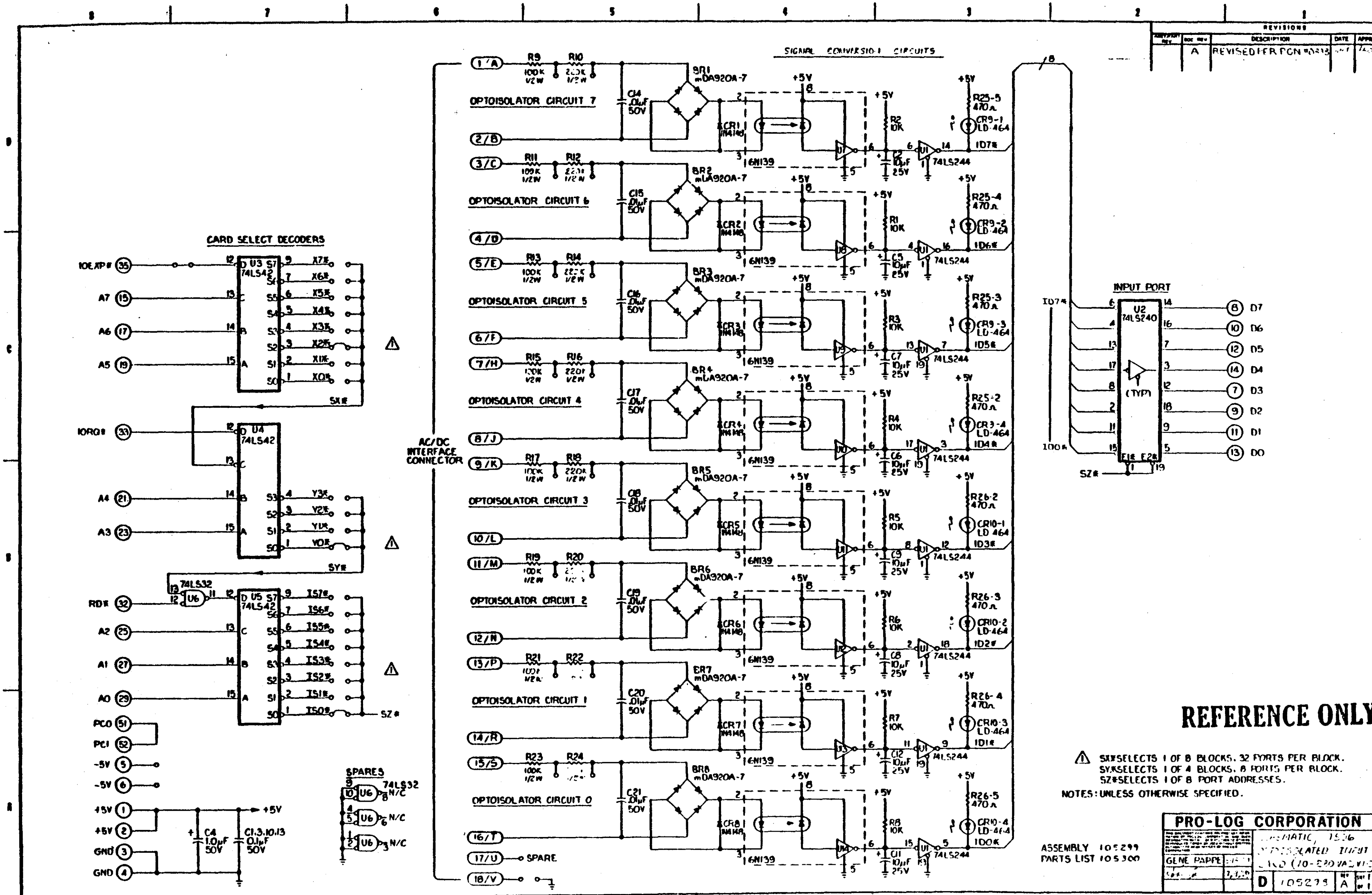
PRO-LOG CORPORATION

ASSEMBLY, 7503 OPTOISOLATOR INPUT CARD (4.5-80 VAC/VDC)

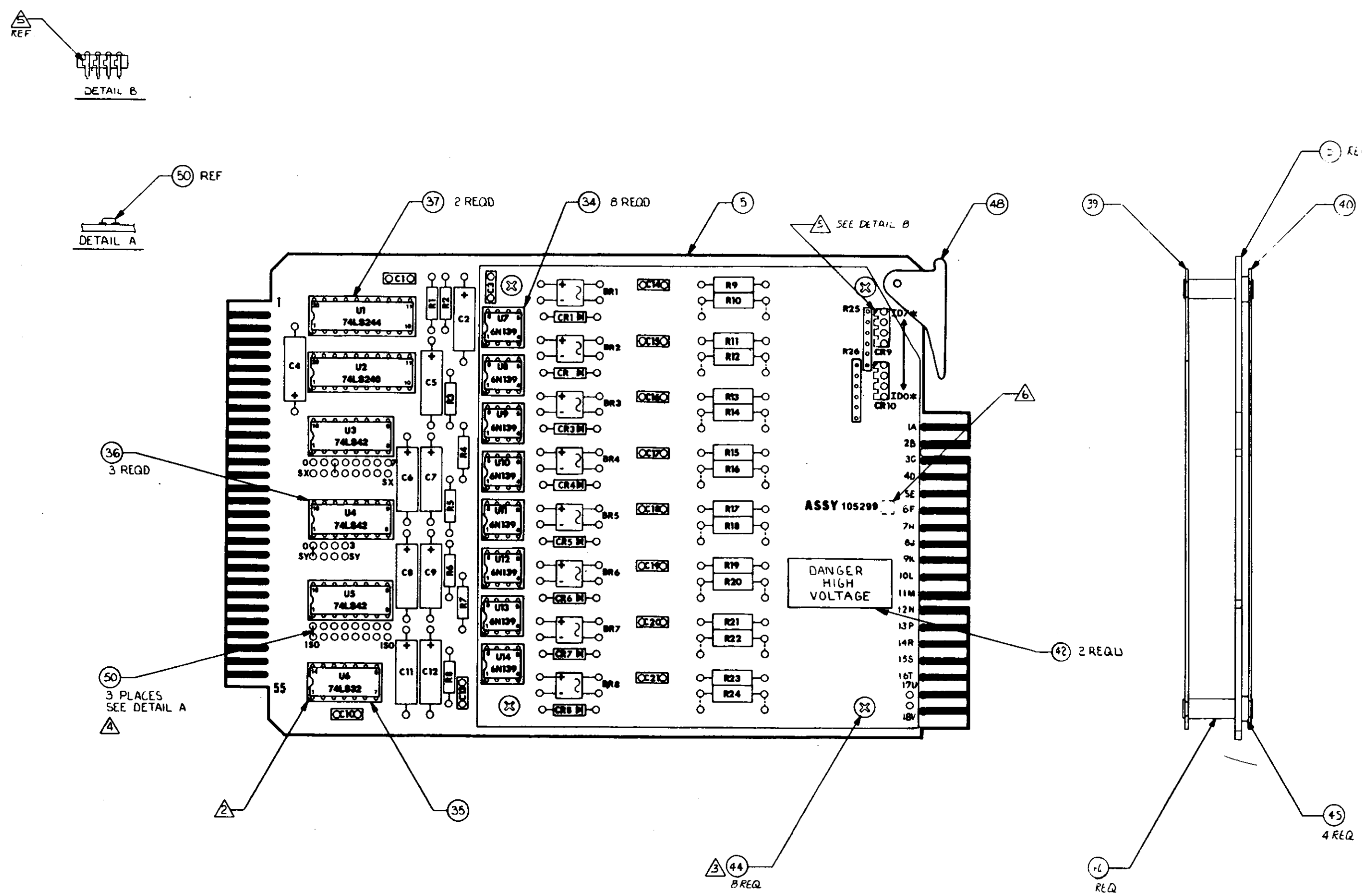
GENE PAPPE

D 105120 REV B SHT 1 OF 1

PRO-LOG


REVISIONS
A REVISED PER PCN #0818
SIGNAL CONVERSION CIRCUITS
CARD SELECT DECODERS
74LS42
74LS32
SPARES
OPTOISOLATOR CIRCUIT 7
OPTOISOLATOR CIRCUIT 6
OPTOISOLATOR CIRCUIT 5
OPTOISOLATOR CIRCUIT 4
OPTOISOLATOR CIRCUIT 3
OPTOISOLATOR CIRCUIT 2
OPTOISOLATOR CIRCUIT 1
OPTOISOLATOR CIRCUIT 0
AC/DC INTERFACE CONNECTOR
mDA920A-7
1N4148
6N139
74LS244
LD-464
INPUT PORT
74LS240
(TYP)
SPARE
REFERENCE ONLY
SX*SELECTS 1 OF 8 BLOCKS, 32 PORTS PER BLOCK.
SY*SELECTS 1 OF 4 BLOCKS, 8 PORTS PER BLOCK.
SZ*SELECTS 1 OF 8 PORT ADDRESSES.
NOTES: UNLESS OTHERWISE SPECIFIED.
ASSEMBLY 105299
PARTS LIST 105300
PRO-LOG CORPORATION
GENE PAPPE
D
A

REV	DOC REV	DESCRIPTION	DATE	APPR
	A	REVISED PER PCN# 3838		



2 INDICATES PIN NO. 1 OF SOCKETS (TYP).

NOTES: UNLESS OTHERWISE SPECIFIED.

1. FOR ASSY PROCEDURES SEE AS1004.
2. INDICATES PIN NO. 1 OF SOCKETS (TYP).
3. APPLY LOCKTITE TO SCREWS.
4. MAPPED TO PORT 40.
5. INDICATES CATHODE PIN OF LED (TYP)
6. IDENTIFY WITH ASSEMBLY REV. LETTER USING RUBBER STAMP.

SCHEMATIC 105298
PARTS LIST 105300

ITEM	DESCRIPTION	REF. DESIGNATION
24	220K,CF,1/2W, 5%	R10,12,14,16,18,20,22,24
23	100K,CF,1/2W, 5%	R9,11,13,15,17,19,21,23
22	470Ω NETWORK	R25-26
21	10K,CF,1/4W, 5%	R1-8
17	MDA920A-7	BR1,2,3,4,5,6,7,8
16		
15	IN4148	CR1,2,3,4,5,6,7,8
14		
13	LD464	CR9, CR10
12		
11	10uF 25V	C2,5-9,11,12
10	1μF 50V	C4
9		
8	.1μF 50V	C1,3,10,13
7	.01μF 50V	C14-21

PRO-LOG CORPORATION

ASSEMBLY, 7506 OPTO-ISOLATED INPUT CARD (90-280 VAC/VDC)

GENE PAPPE

D | 105299 | REV A | SHT 1 OF 1

PRO-LOG

USER'S MANUAL

PRO-LOG
CORPORATION

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Monterey, California 93940
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